AT

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/661,187	09/13/2000	Eiji Oishi	9319S-000161	8015

7590 02/23/2005

Harness Dickey & Pierce PLC
P O Box 828
Bloomfield Hills, MI 48303

EXAMINER	
SEMENENKO, YURIY	
ART UNIT	PAPER NUMBER
2841	

DATE MAILED: 02/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/661,187	OISHI ET AL.	
	Examiner	Art Unit	
	Yuriy Semenenko	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *1/102005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) *10,11 and 16* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9 and 12-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *1-16* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 September 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2 pages 1/22/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1.1. Applicant's election with traverse of Group I claims 1-9 and 12-15 drawn to composite flexible wiring board in the reply filed on 1/10/2005 is acknowledged.
The traversal is on the ground(s) that: "... all groups of claims are sufficiently related to each other that an undue burden would not be placed upon the Examiner by maintaining all groups in a single application. "

This is not found persuasive because:
Although the inventions all groups are related to each other, but inventions are distinct, as explained in letter of Restriction and /or Election, filing date 12/28/04. Therefore, no further explanation or proof is necessary. The election of one invention following a requirement for restriction is mandatory even though applicant disagrees with the examiner.

The requirement is still deemed proper and is therefore made FINAL.

1.2. Upon indication of allowable subject matter, any claim containing such subject matter will be rejoined and allowed.

Priority

2. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the

subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3.1. Claims 1-9, 12-14 are rejected under 35U.S.C. 103(a) as being obvious over Y. Tagusa et al. (Patent #5668700) hereafter Tagusa in view of J.J. Stopperan (Patent # 5719749) hereafter Stopperan.

3.1.1. Regarding claim 1: Tagusa discloses a composite flexible wiring board (Fig. 3) comprising first flexible wiring board 2 and second wiring board 13. The second wiring board 13 is provided on the first flexible wiring board 2 in predetermined area (see Fig. 3). The first flexible wiring board and the second wiring board are electrically connected to each other through an interlayer contact portion 8b (Fig. 3) provided in a predetermined position.

But Tagusa does not teach that the second wiring board is a flexible wiring board on which a surface-mounted part is mounted.

Stopperan discloses a composite flexible wiring board (Fig. 1, 2) comprising first flexible wiring board 42 and second flexible wiring board 52 on which a surface-mounted part 70 is mounted. The first flexible wiring board and the second flexible wiring board are electrically connected to each other through an interlayer contact portion 74 (Fig. 2).

At the time the invention was made, it was well know to use composite flexible wiring boards for electronic devices and to mount on it (flexible wiring board) the surface-mounted part.

Therefore, it would have been obvious to one of ordinary skill in the art, at time the invention was made, for Tagusa to make the second wiring board a flexible wiring board on which a surface-mounted part is mounted, as taught by Stopperan, to provide increased packing density.

3.1.2. Regarding claim 2: Tagusa further discloses as discussed above with respect to claim 1 a second flexible wiring board 13 (Fig. 3) of the composite flexible wiring board arranged on part the first flexible wiring board 2 (see Fig.3,).

3.1.3. Regarding claim 3: Tagusa, as modified, discloses in Fig. 3 the composite flexible wiring board according to claim 1. At least a power IC chip 1 is mounted on the first flexible wiring board 2.

3.1.4. Regarding claim 4: Tagusa, as modified, discloses the first flexible wiring board 40 (Fig. 1, 4) has an input terminal region 5f and an output terminal region 5e (column 10, lines 53-67).

3.1.5. Regarding claim 5: Tagusa, as modified, discloses the composite flexible wiring board having all of the claimed features as discussed above with respect claims 1, except he doesn't teach the second flexible wiring board includes at least one kind surface-mounted part selected from among flat-packaged LSI, a resistor, a capacitor, an inductance, a diode, a transistor, a quartz oscillator, and connector. Stopperan discloses (column 5, lines 29-35) the second flexible wiring board 52 includes at least one kind surface-mounted part 70, 71 (Fig. 1) selected from among flat-packaged LSI, a resistor, a capacitor, an inductance, a diode, a transistor, a quartz oscillator, and connector.

At time the invention was made, it was well known to include in the second flexible wiring board one kind of surface-mounted part selected from among flat-packaged LSI, a resistor, a capacitor, an inductance, a diode, a transistor, a quartz oscillator, and connector. Therefore it would have been obvious to one of ordinary skill in the art, at time the invention was made, for Tagusa to include in his invention that the second flexible wiring board includes at least one kind surface-mounted part selected from among flat-packaged LSI, a resistor, a capacitor, an inductance, a diode, a transistor, a quartz oscillator, and connector as, taught by Stopperan to provide miniaturization of device.

3.1.6. Regarding claim 6: Tagusa, as modified, discloses in Fig. 3 the composite flexible wiring board 41 according to claim 3. The power IC chip 1 (Fig. 3) is connected to an conductive layer 7 of the first flexible wiring board 2 through an anisotropic conductive film 8.

3.1.7. Regarding claim 7: Tagusa, as modified, discloses in Fig. 3 the composite flexible wiring board having all of the claimed features as discussed with respect claims 1. As discussed above with respect to claim 1, Stopperan discloses a surface-mounted part 70 mounted on second flexible wiring board 40 (Fig. 2).

However, he doesn't teach the surface-mounted part connected to an conductive layer 68 through a solder layer. Tagusa teaches (column 11, lines 40-63 and column 12, lines 7-8) the surface-mounted part 1 (Fig. 3) is connected to an conductive layer 7 through a solder 8c and 8d.

At time the invention was made, it was well known to use a solder layer for connection of a surface-mounted part to a substrate. Therefore it would have been obvious to one of ordinary skill in the art, at time the invention was made, for Stopperan to include in the invention the surface-mounted part connected to an conductive layer of the second flexible wiring board, through a solder layer to provide better connection.

3.1.8. Regarding claim 8: And furthermore Tagusa, as modified, discloses in Fig. 3 the composite flexible wiring board as discussed above with respect to claim 1 with the interlayer contact portion 8b constituted by an anisotropic conductive film or solder (claims 3 and 4, column 12, lines 62-67).

3.1.9. Regarding claim 9: Tagusa, as modified, discloses in Fig. 3 the composite flexible wiring board having all of the claimed features as discussed above with respect claims 1. The first flexible wiring board 40 (Fig. 1) has an output terminal region 5e (the output side wiring line 5a in Fig. 5 and column 10, lines 53-67).

However, he doesn't teach that the composite flexible wiring board comprises another flexible wiring board connected to the first flexible wiring board and the another first flexible wiring board having an output terminal region.

Stopperan discloses in (Fig. 1, 2) the composite flexible wiring board further comprising another flexible wiring board 22 connected to the first flexible wiring board 42 having an output terminal region 12.

Therefore it would have been obvious to one of ordinary skill in the art, at time the invention was made, for Tagusa to includes in the invention the composite flexible wiring board further comprising another flexible wiring board connected to the first flexible wiring board and the another first flexible wiring board having an output terminal region. The benefit of doing so

would be to provide connection the composite flexible wiring board to electro-optical panel with high packing density.

3.1.10. Regarding claim 12: Tagusa discloses in Fig. 3 electro-optical device comprising an electro- optical panel 9 including at least one substrate 9a,which has a wiring junction region 12. The wiring junction region 12 is connected to the composite flexible wiring board 41.

However, he does not teach that the second wiring board is flexible wiring board according claim 1. Stopperan teaches a composite flexible wiring board having all of the claimed features as discussed above with respect claims 1.

At time the invention was made, it was well know to use composite flexible wiring boards for electronic devices. Therefore it would have been obvious to one of ordinary skill in the art, at time the invention was made, for Tagusa to includes in his invention the electro-optical device comprising an electro-optical panel connected to a composite flexible wiring board according claim1, as taught by Stopperan to increase packaging density.

3.1.11. Regarding claim 13: Tagusa, as modified, discloses in Fig. 3 an electro-optical device having all of the claimed features as discussed above with respect claims 12. The electro-optical panel includes first substrate 9a and second substrate 9b arranged in opposite relation to face each other. The first substrate 9a has wiring junction region 12 not superimposed with the second substrate.

3.1.12. Regarding claim 14: Tagusa, as modified, discloses in Fig. 3 an electro-optical device having all of the claimed features as discussed above with respect claims 13. The electro-optical panel includes a liquid crystal layer 11 disposed as an electro-optical material layer between the first substrate 9a and the second substrate 9b.

3.2. Claim 15 is rejected under 35U.S.C. 103(a) as being obvious over Tagusa in view of Stopperan as applied to claim 12 and in further view of Y. Hirakata et. al. (Patent #6005645) hereafter Hirakata.

Tagusa, as modified, discloses in Fig. 3 an electro-optical device having all of the claimed features as discussed above with respect claims 12. The electro-optical device comprises an electro-optical panel 9.

However he does not teach that the electro-optical panel is an EL display panel including, as an electro-optical material layer, an electroluminescence structure formed on the substrate.

Hirakata teaches (column 3, lines 24-41) that an electro-optical panel can be an EL display panel including an electroluminescence structure formed on substrate 9a.

At time the invention was made, it was well know to use an electroluminescence structure as an electro-optical material layer. Therefore it would have been obvious to one of ordinary skill in the art, at time the invention was made, for Tagusa to includes in his invention an electro-optical device comprising an electro-optical panel, which is an EL display panel including, as an electro-optical material layer, an electroluminescence structure formed on said substrate, as taught by Hirakata et al. The motivation for doing so would be provided by the suggestion at column 1, line 24 of Tagusa et al to use one of these display devices in the panel.

4.1. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yuriy Semenenko whose telephone number is (571) 272-6106. The examiner can normally be reached on 8:30am - 5:00pm.

4.2. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on (571)- 272-1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

4.3. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

YS

Vit Miska
Primary Examiner